FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NPO-20773-1-CU Serial No.: 10/061,066

Applicant(s): Adrian Stoica

Filing Date: January 29, 2002 Group: 2133

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

U. S. PATENTS

Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
CVL	US-5,258,947	11-02-1993	SOURGEN	365	96	12-07-1990
CVL	US-6,363,519	03-26-2002	LEVI ET AL.	716	16	06-17-1999

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)

Examiner's Signature: [signature] Date Considered: 9/9/05

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U. S. PATENTS

Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
CVL	5,677,691	10-14-07	HOSTICKA ET AL.	341	155	06-25-93
CVL	5,705,938	01-06-98	KEAN	326	39	09-05-95
CVL	5,959,871	09-28-99	PIERZCHALA ET AL.	364	489	12-22-94
CVL	5,970,487	10-19-99	SHACKLEFORD ET AL.	707	6	08-13-97
CVL	6,360,191	03-19-02	KOZA ET AL.	703	6	01-05-99
CVL	6,363,517	03-26-02	LEVI ET AL.	716	16	06-17-99
CVL	6,378,122	04-23-02	LEVI ET AL.	716	16	06-17-99

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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
CVL	Layzell, P., "A New Research Tool for Intrinsic Hardware Evolution", 1998, Second International Conference ICES98 , pp. 47-56
CVL	Perkowski, M., Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints," July 1999, Proceedings of the First NASA/ DoD Workshop
CVL	Stoica, Adrian, "Toward Evolvable Hardware Chips: Experiments with a Programmable Transistor Array," April 1999, Proceedings of the Seventh International Conference
CVL	Stoica, A., Keymeulen, D., Salazar-Lazaro, C., Hayworth, K., and Tawel, Raoul, "Toward On-board Synthesis and Adaption of Electronic Functions: An Evolvable Hardware Approach," March 1999, IEEE, Vol. 2, pp. 351-357
CVL	Stoica, A., Keymeulen, D., Tawel, R., Salazar-Lazaro, C., and Li, W., "Evolutionary experiments with a fine-grained reconfigurable architecture for analog and digital CMOS circuits," July 1999, Proceedings of the First NASA/DoD Workshop,
CVL	Stoica, A., Klimeck, G., Salazar-Lazaro, C., Keymeulen, D., and Thakoor, A., "Evolutionary Design of Electronic Devices and Circuits," July 1999, IEEE, Vol. 3, pp. 1271-1278

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INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO - 1449)	Docket No.: NP0-20773-1-CU Serial No.: To be assigned Applicant(s): STOICA Filing Date: Herewith Group: Unknown

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Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
CVL	5,867,397	02-02-99	KOZA, et al.	364	489	
CVL	5,897,628	04-27-99	KITANO	706	13	

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CVL	Bennett III, F., Andre, D., Koza, J.R., and Keane, M.A., "Evolution of a 60 decibel Op Amp using genetic programming," First International Conference, *ICES96*, Tsukuba, Japan, October, 7-8, 1996, Springer, pp. 455-469
CVL	Flockton, Stuart, J., and Sheehan, Kevin, "Intrinsic Circuit Evolution Using Programmable Analogue Arrays," Second International Conference, *ICES98*, Lausanne, Switzerland, September 23-25, 1998, Springer, pp. 144-153.
CVL	Iba, H., Iwata, M. and Higuchi, T., "Machine Learning Approach to Gate-Level Evolvable Hardware," First International Conference, *ICES96*, Tsukuba, Japan, October 7-8, 1996, Springer, pp. 327-343.
CVL	Kajitani, I., Hoshino, T., Nishikawa, D., Yokoi, H., Nakaya, S., Yamauchi, T., Inuo, T., Kajihara, N., Iwata, M., Keymeulen, D., Higuchi, T., "A Gate-Level Ettwchip: Implementing GA Operations and Reconfigurable Hardware on a Single LSI," Second International Conference, *ICES98*, Laussane, Switzerland, September 23-25, Springer, pop. 1-12.
CVL	Koza, J.R., Andre, D., Bennett III, F., Keane, M.A., "Reuse Parameterized Reuse, and Hierarchical Reuse of Substructures in Evolving Electrical Circuits Using Genetic Programming, "First International Conference, *ICES96*, Tsukuba, Japan, October 7-8, 1996, Springer, pp. 312-325.

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CVL	Koza, J.R., Bennett III, F.H., Andre, D., Keane, M.A., "Automated WYWIWYG Design of Both the Topology and Component Values of Electrical Circuits Using Genetic Programming," *Proceedings of Genetic Programming Conference*, Stanford, 1996, pp. 28-31.
CVL	Koza, J.R., Dunlap, F., Bennett III, F., Keane, M.A., Lohn, J., and Andre, D., "Automated Synthesis of Computational Circuits Using genetic Programming," *IEEE Transactions on Evolutionary Computation*, Vol. 1, No. 2, 1997, pp. 109-128.
CVL	Lohn, Jason D., and Colombano, S.P., "Automated Analog Circuit Synthesis Using a Linear Representation," Second International Conference, *ICES98*, Lausanne, Switzerland, September 23-25, Springer, 1998, pp. 125-133.
CVL	Murakawa, M., Yoshizawa, S., Adachi, T., Suzuki, S., Takasuka, K., Iwata, M., Higuchi, T., "Analogue EHW Chip for Intermediate Frequency Filters," Second International Conference, *ICES98*, Lausanne, Switzerland, September 23-25, 1998, Springer, pp. 132-143.
CVL	Stoica, A., "On Hardware Evolvability and Levels of Granularity," *International Conference on Intelligent Systems and Semiotics*, NIST Gaithersburg, VA, September 1997, pp. 1-4.
CVL	Thompson, Adrian, "Silicon Evolution," *Proceedings of Genetic Programming, MIT Press*, 1996, pp. 75-90.
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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
CVL	Thompson, Adrian, "An Evolved Circuit, Intrinsic in Silicon, Entwined with Physics," First International Conference, *ICES96*, Tsukuba, Japan, October 7-8, Springer, 1996, pp. 390-405.
CVL	Zebulum, R.S., Pacheco, M.A., Vellasco, M., "Evolvable Systems in Hardware design: Taxonomy, Survey and Applications," First International Conference, *ICES96*, Tsukuba, Japan, October 7-8, Springer, 1996, pp. 344-358.
CVL	Zebulum, R.S., Pacheco. Marco, A., Vellasco, M., "Analog Circuits Evolution in Extrinsic and Intrinsic Modes," Second International Conference, *ICES98*, Lausanne, Switzerland, September 23-25, Springer, 1998, pp. 154-165.

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